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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,093	09/12/2003	Jeffrey D. Gilbert	42P17020	8868

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INTEL CORPORATION
c/o INTELLEVATE, LLC
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,093	GILBERT ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-31 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-31 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 16, 2007 has been entered.

2. Claims 1, 3-31 and 33 remain pending.

Response to Arguments

3. Applicant's arguments filed on October 3, 2007 have been fully considered but they are not persuasive.

a. Applicants argue on page 9, paragraph 1 of the remarks that "the WO reference does not teach a cache line having two cache coherency states. The cache line cannot have both the 'E' state and the 'M' state at the same time".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a cache line having two cache coherency states at the same time) are not recited in the rejected claim(s). Although the claims are interpreted in light of

the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The claim simply recites, inter alia, "a cache accessible from a first interface and a second interface, to contain a cache line, the cache line having two cache coherency states with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface, wherein said first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor".

The WO reference unequivocally discloses the claimed invention in Fig. 1 where a cache (CS) accessible by a plurality of processors (EPs) through a first interface (BS1) on one side and accessible by additional cache memories, main memory (MEM), or all types of I/O through a second interface (BS2). If a line was recently cached from main memory (MEM) through BS2, said cache line is in the exclusive state, and if one of the processors (EPs) wants to read the cache line, and performs some operation that require changing the state of the cache to modified, another associated processor (EP) trying to read the same cache line through interface BS1 would find it in a modified state; See Fig. 1, p. 6 et seq.

Furthermore, WO discloses "requests can be made between the additional cache memories CS and the individual processors EP (through interface BS1 processors EP guarantee access of a cache line with a first coherency state), and requests between additional cache memories CS and the main memory

(through cache memory bus BS2 guarantee accessing a cache line with a second coherency state); p.7, par. 4.

Additionally, the WO reference discloses in Fig. 3 a state diagram having the expanded states SI, ES, MI, MS, II, SS, EM, and MM, the first letter of a state title relating to the state in the TLC, while the second letter relates to the state in the SLC and/or in a lower cache hierarchy state; See Page 12.

b. Applicants further argue on page 9, paragraph 2 of the remarks that the WO reference does not teach or suggest that "EP accesses a cache line in the CS using one of the two coherency states of the cache line because a cache line in the CS has only one coherency state at one time and there are no two cache coherency states associated with a cache line at the same time".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., two cache coherency states associated with a cache line at the same time) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The WO reference unequivocally discloses in Fig. 3 a state diagram having the expanded states SI, ES, MI, MS, II, SS, EM, and MM, the first letter of

a state title relating to the state in the TLC, while the second letter relates to the state in the SLC and/or in a lower cache hierarchy state; See Page 12.

c. Applicants argue on page 10, paragraph 2 of the remarks that "the expanded states are not two coherency states for a cache line in the same cache".

Examiner respectfully disagrees. The WO reference clearly shows single MESI TLC state (e.g., I, S, E, M) and single MESI SLC state (e.g., I, S, E, M) transitioning to joint coherency state (e.g., SI, ES, EM, MI, MI, MS...). The WO reference further shows a state diagram having the expanded states SI, ES, MI, MS, II, SS, EM, and MM, the first letter of a state title relating to the state in the TLC, while the second letter relates to the state in the SLC and/or in a lower cache hierarchy state; See Fig. 3; Page 12.

d. Applicants argue on page 13, paragraph 1 of the remarks that "the WO reference does not teach or suggest the limitation of transitions from a single coherency state to a joint coherency state".

Examiner respectfully disagrees. The WO reference clearly shows single MESI TLC state (e.g., I, S, E, M) and single MESI SLC state (e.g., I, S, E, M) transitioning to joint coherency state (e.g., SI, ES, EM, MI, MI, MS...). The WO reference further shows a state diagram having the expanded states SI, ES, MI,

MS, II, SS, EM, and MM, the first letter of a state title relating to the state in the TLC, while the second letter relates to the state in the SLC and/or in a lower cache hierarchy state; See Fig. 3; Page 12.

Claim Rejections - 35 USC § 103.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-10, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,629,268) in view of WO 00/52582 and further in view of Arimilli (2002/0129211).

As per claim 1, Arimilli (6,629,268) discloses an apparatus, comprising: a first interface [Fig.2; Bus Interface Unit 35]; a second interface not directly coupled to said first interface [Fig.2; Interface 18]; and a cache accessible from said first interface and said second interface [Fig.2; L2 cache, Bus Interface 35, Interface 19; col.8, lines 6-33].

However, Armilli (268) does not specifically teach a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface as required.

WO 00/52582 discloses a cache containing a cache line, the cache line having two cache coherency states, with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface [Fig. 1; page 11, ll 16-32; page 12, ll 21-27; Fig. 3; Page 12] to increase the performance capability of processor systems while ensuring that the cache memory block is not read unnecessarily (page 1, ll 1-5; page 11, ll 18-23).

Since the technology for implementing a cache memory system with a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface was well known as evidenced by WO 00/52582, an artisan would have been motivated to implement this feature in the system of Arimilli (268) in order to increase the performance capability of processor systems while ensuring that the cache memory block is not read unnecessarily. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Arimilli (268) to include a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface since this would have increased the performance capability

of processor systems while ensuring that the cache memory block is not read unnecessarily (page 1, ll 1-5; page 11, ll 18-23) as taught by WO 00/52582.

Arimilli (268) and WO disclose the claimed invention as discussed above in the previous paragraphs. However, Arimilli (268) and WO do not specifically teach the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor as required by the claims.

Arimilli (2002/0129211) discloses the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor [par. 10] to resolve conflicts between requests to modify a cache line (par. 2).

Since the technology for implementing a cache system with the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor was well known as evidenced by Arimilli (211), an artisan would have been motivated to implement this feature in the system of Arimilli (268) and WO in order to resolve conflicts between requests to modify a cache line. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Armilli (268) and WO to include the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor because this would have resolved conflicts between requests to modify a cache line (par. 2).

As per claim 31, the rationale in the rejection of claim 1 is herein incorporated. Arimilli (268) further discloses a bus bridge to a third interface [Fig.1]; and an input-output device coupled to a third interface [Fig.3].

As per claim 3, Arimilli (211) discloses a second cache coherency state is to reduce snoop transactions on said second interface [par. 5].

As per claim 4, Arimilli (211) discloses said first cache coherency state is exclusive and said second cache coherency state is shared [pars. 6, 24 and 36].

As per claim 5, Arimilli (211) discloses first cache coherency state is modified and said second cache coherency state is shared [par. 8].

As per claim 6, Arimilli (211) discloses second cache coherency state supports speculative invalidation [par. 6].

As per claim 7, Arimilli (211) discloses first cache coherency state is modified and said second cache coherency state is invalid [par. 7].

As per claim 8, Arimilli (211) discloses first cache coherency state is exclusive and said second cache coherency state is invalid [pars. 6 and 36].

As per claim 9, Arimilli (211) discloses the first cache coherency state is shared and said second cache coherency state is invalid [par. 7].

As per claim 10, Arimilli (211) discloses the second cache coherency state further supports explicit invalidation [pars. 7 and 10].

As per claim 33, the rationale in the rejection of claim 3 is herein incorporated.

6. Claims 11-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (2002/0129211) in view of WO 00/52582.

As per claim 11, Armilli (211) discloses a method, comprising: associating a first cache coherency state with a first cache line in a first cache [par. 10]; associating a second cache coherency state with a second cache line in a second cache coupled to said first cache via said second interface [pars. 24 and 29];

However, Arimilli (211) does not specifically teach transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces; and transitioning a second cache coherency state to a third cache coherency state as required by the claim.

WO 00/52582 discloses transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for said first interface and

a third cache coherency state for said second inteface, said first cache coupled to a first interface and to a second interface [Fig. 3; page 7, ll 27 to page 8, ll 13; page 15; ll 1-19]; and transitioning a second cache coherency state to a third cache coherency state [Fig .3; page 15, ll 15-19] to allow the cache to have a deeper knowledge about the state situation within the processor system, which allows it to relay and/or capture requests directed to the individual processors (page 15, ll 22-25).

Since the technology for implementing a cache system with transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces was well known as evidenced by WO 00/52582, an artisan would have been motivated to implement this feature in the system Arimilli (211) since this would have allowed the cache to have a deeper knowledge about the state situation within the processor system, which allows it to relay and/or capture requests directed to the individual processors. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Arimilli (211) to include transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces in order to the cache to have a deeper knowledge about the state situation within the processor system, which allows it to relay and/or capture requests directed to the individual processors (page 15, ll 22-25) as taught by WO 00/52582.

As per claim 12, WO 00/52582 discloses a first cache coherency state is

exclusive, a second cache coherency state is invalid, and a third cache coherency state is shared [Fig. 3].

As per claim 13, WO 00/52582 discloses a first cache coherency state is modified, said second cache coherency state is modified, and said third cache coherency state is invalid [Fig. 3].

As per claim 14, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 15, Arimilli (211) discloses the first cache coherency state is modified [par. 36].

As per claim 16, Arimilli (211) discloses the first cache coherency state is exclusive [par. 36].

As per claim 17, Arimilli (211) discloses the first cache coherency state is shared [par. 37].

As per claim 18, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 19, WO 00/52582 discloses the first cache coherency state is invalid and the joint cache coherency state is exclusive-shared [Fig. 3].

As per claim 20, WO 00/52582 discloses the first cache coherency state is modified-invalid and the joint cache coherency state is modified-shared [Fig. 3].

As per claim 21, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 22, the rationale in the rejection of claim 12 is herein incorporated.

As per claim 23, the rationale in the rejection of claim 13 is herein incorporated.

As per claim 24, the rationale in the rejection of claim 14 is herein incorporated.

As per claim 25, the rationale in the rejection of claim 15 is herein incorporated.

As per claim 26, the rationale in the rejection of claim 16 is herein incorporated.

As per claim 27, the rationale in the rejection of claim 17 is herein incorporated.

As per claim 28, the rationale in the rejection of claim 18 is herein incorporated.

As per claim 29, the rationale in the rejection of claim 19 is herein incorporated.

As per claim 30, the rationale in the rejection of claim 20 is herein incorporated.

Conclusion

7. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art

disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

9. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

October 28, 2007

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
10/29/07

Mardochee Chery
Examiner
AU: 2188